| **SYNOPSIS : MINI PROJECT 2-A-2023-24** | | |
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| **PROJECT NAME (Group Number )** | | **FPGA Based Smart Voting System** |
| **ELECTRONICS AND TELECOMMUNICATION ENGINEERING** | | |
| **Vivekanand Education Society's Institute of Technology** | | |
| **Student’s Name (Class /Roll Number)** | | Manish Mhatre (D14B/33) |
| **Student’s Name (Class /Roll Number)** | | Vedant Patil (D14B/47) |
| **Student’s Name (Class /Roll Number)** | | Rushikesh Sarak (D14B/53) |
| **Mentor Name** | | Dr.Nandini Ammanagi |
| **Sem/Year/CAY** | | V/TE/2023-24 |
| **Problem Statement** | Design and implement FPGA Based Smart Voting System . | |
| **Objectives** | 1. To study and learn working and applications of Verilog and FPGA boards. 2. Implement a smart voting system which can authenticate users based on documents for votes. 3. Design and develop an accurate vote tracking and managing system with great precision. 4. The smart voting machine can automatically maintain the data log of vote in encrypted format. | |
| **SPECIFIC:** | The aim of this project is to implement and design a smart voting system which authenticates votes based on biometric or voting essential documents and also manages the collected votes in a precise manner . Our team includes 3 members Manish Mhatre, Rushikesh Sarak, Vedant Patil. The project is divided and the following tasks are assigned to each member:   * Procurement of components and design: Rushikesh Sarak, Manish Mhatre, Vedant Patil, . * Software simulation : Rushikesh Sarak, Manish Mhatre. * Troubleshooting : Rushikesh Sarak, Manish Mhatre, Vedant Patil.   This project will be finished before April and remaining time can be utilized for troubleshooting and project report. | |
| **MEASURABLE:** | We will develop a smart voting system to authenticate voters and also tracking vote log with great precision to implement the voting process efficiently with precision. | |
| **ACHIEVABLE:** | For this project Vivado HLX is required. | |
| **RELEVANT:** | By designing and implementing a smart voting system, the project aims to implement elections on a small scale efficiently and effectively. | |
| **TIME-BOUND** | Components procuring : 1-February -2024  Software simulation : 8-February-2024  Troubleshooting : 16-March-2024  Final Report : 5-April -2024 | |
| **S.M.A.R.T Goal** | We aim to develop a “Smart Voting System” to conduct election voting at small scale effectively and precisely. | |
| **Introduction :**  In democracy electing a right person through your vote is essential.In everyday life we came across situation where we have to elect the right person for different posts,the single vote casted can have ability to create difference.Therefore process of election should be conduct properly.The ‘smart voting system’ is made for conducting local small-scale elections where implementing the system manually through human means is challenging and troublesome-some and use of advance machinery would be costly.Firstly it authenticates the user through biometric and document-ID.In case of valid voter only it initializes process of voting.The system is designed to provider accurate vote counts data by avoiding mal-practices done by user like pressing two buttons at a time or pressing any button more than given time. The track of votes are taken by system through counter arrangement. The final data collected are maintained by the system and can be only accessible for special users having the access.The whole process of voting system is tracked by a system in case of any discrepancy the system will boot itself and set to default to avoid any error in voting.  **Description :**  The ‘smart voting system’ is developed to implement a small scale election effectively and efficiently.The system is developed to authenticate the voters who are going to cast their precious votes on a voting system that not only avoid bogus voting but also avoid unfair-means of voting. The casted votes are collected and stored in encrypted data form which becomes nearly impossible to decode for invader.The data log of collected votes are maintained by the system and can be only accessible for special users having the access. The whole process of the voting system is tracked by a system in case of any discrepancy the system will boot itself and set to default to avoid any error in voting. The FPGA frame-work used provides a flexible and reliable frame-work to set the voting system based on the scenario ,further this system can be changed easily as per user’s requirement.    **Fig 1 Block diagram of Smart Voting system** | | |
| **Subject Teacher : Dr. Nandini Ammanagi**  **Date :**  **Signature :** | | |